

FET62xx-C SoM

The FET62xx-C is a cost efficient and advanced performance System on Module (SoM) based on TI Sitara™ AM62x series industrial grade SoCs powered by ARM Cortex A53 cores with speed up to 1.4GHz. The FET62xx-C SoM is integrated with a wide array of interfaces such as 2-port Gigabit Ethernet, TSN,USB 2.0, MMC/SD, Camera interface, OSPI, CAN-FD. With the pin-to-pin compatibility for single-core AM6251, dual-core AM6252 and quad-core AM6254, the FET62xx-C SoM is an ideal solution for designers to short time-to-market, and could be used in a wide range of industrial applications, such as Human Machine Interfaces (HMI), Industrial computer, Edge computing, Retail automation, Telematics Control Unit (TCU), 3D Re-configurable automotive instrument cluster, Medical equipment.



4x A53	1.4GHz	8G FLOPS	
Architecture	Clock	GPU	
TSN	16nmFF	64-bit	
Ethernet	Technology	Processor	



Linux5.10

Features:

- 10~15 years lifespan;
- Cortex-A53+Cortex-M4F, more secure;
- Support IEEE1588 PTP(Precision Time Protocol);
- 2x 1000Mbps Ethernet(GMAC), support TSN;
- Supports RGB 888, LVDS, up to 1920 x 1200@60fps。

SoM features :

CPU	TI AM62x				
	MPU: Cortex-A53 @1.4GHz				
	MCU: Cortex-M4F @400 MHz				
	GPU:				
	•AXE1-16M@500MHz				
	•OpenGL 3.x/2.0/1.1 + Extensions, Vulkan 1.2				
RAM	1GB/2GB DDR4				
ROM	8GB eMMC				
Voltage input	DC 5V				
Operating	-40~85℃				
temp					
Package	Board-to-board connector(4*80-pin, 0.5mm pitch)				

Note: NPU is not available.

AM62x series processor

Item	AM6254	AM6252	AM6251	AM6234	AM6232	AM6231
CPU core number	4	2	1	4	2	1
3D Graphics engine	√	√	√	×	×	×

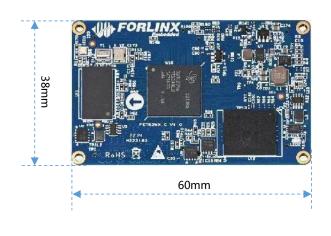
SoM parameters:

A53 interface	QTY	Spec.
		2x 4-lane LVDS(8 data,2clocks), each lane up to 1.19 Gbps; Single LVDS up to WUXGA(1920x1200@60fps, 162MHz pixel clock);
LVDS*a	2	Supports three modes as below:
,,	_	•single LVDS output model;
		•2x single LVDS(copy) output mode: two LVDS output same content;
		•dual LVDS output mode, 8-lane data and 2-lane clock combine to one output channel
RGB Parallel*a	1	One RGB888 parallel interface, up to WUXGA(1920 x 1200@60fps, 165MHz pixel clock)
		One 4-lane MIPI CSI;
MIPI CSI	1	MIPI-DPHY 1.2;
		Supports 1, 2, 3 or 4-lane mode, each lane up to 2.5Gbps;
		Sending and receiving clock up to 50MHz;
Audio	≤3	Supports TDM, Inter-IC Sound(I2S) and other similar forms;
		Supports digital audio (SPDIF, IEC60958-1 and AES-3);
		Supports audio reference output clock
SD	≤2	Supports two 4-bit SD/ SDIO, up to UHS-I;
		Complies with eMMC 5.1, SD 3.0 and SDIO3.0
		Supports RMII(10/100) or RGMII(10/100/1000);
Ethernet	2	Supports IEEE1588(Annex D, Annex E, Annex F with 802.1AS PTP);
Ethernet	2	Supports TSN;
		Supports hardware IP/UDP/TCP verify and uninstall
		USB 2.0(up to 480 Mbps);
USB	2	Can be configured to USB host, USB device or USB DRD(dual-role device) mode;
		Integrated with USB VBUS
		Compatible with 16C750;
		Supports RS485 flow control;
UART	≤9	Rating up to 3.6Mbps;
		Stop bit is available for 1, 1.5, 2bit;
		Check bit: odd, even, none
		Complies with CAN2.0A, B or ISO 11898-1
CAN-FD	-2	Supports complete CAN FD(up to 64 data bytes)
CAN-FD	≤3	Supports RAM parity check/ ECC
		Rating up to 5Mbps
SPI		Each lane has programmable frequency, pole and polarity and phase of serial clock;
	≤5	MCSPI up to 50MHz
120	-/(Support standard mode(up to 100Kbps) and high speed mode(400Kbps);
I2C	≤6	7-bit and 10-bit device addressing mode
		Each pair of PWM support two PWM output(EPWMxA and EPWMxB) available for below
PWM	≤3	configuration:
		•two separate PWM output, single edge;

		•two bilaterally symmetrical separate PWM;
		•one bilateral asymmetry separate PWM output ;
		•Dead-band generation with independent rising and falling edge delay control
		Enhanced quadrature encoder pulse input;
eQEP		•input sync;
	≤3	•quadrature encoder unit;
		•Supports position counters and control units for position measurement
		•Supports quadrature edge capture unit for low-speed measurements
		Enhanced capture module, applicable for
		•audio input sampling rate measurement;
-CAD		•rotating machinery speed measurement(eg. Toothed sprockets sensed by Hall sensors);
eCAP	≤3	•Elapsed time measurement between position sensor pulses;
		•Period and duty cycle measurement of pulse train signals;
		•Decode current or voltage magnitude from duty cycle encoded current/voltage sensors
GPMC		Up to 133MHz
	1	Flexible 8-bit and 16-bit asynchronous memory interface, can be mounted with
	1	maximum4chips(22-bit address);
		Available for NAND, NOR, Muxed-NORand SRAN
OSPI/QSPI	1	Supports 166MHz DDR/200MHz SDR
JTAG	1	Supported

a. Available for 1 x 2048x1080 + 1 x 1280x720

Exterior and dimensions:







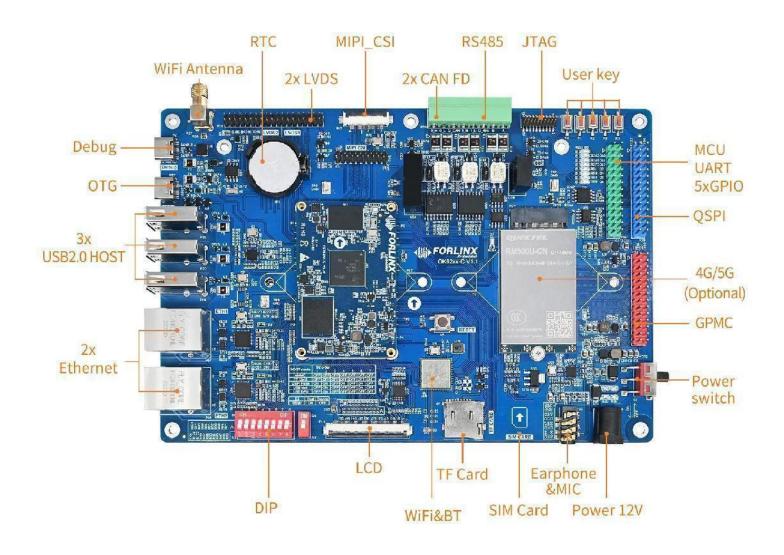
Height diagram after installation

*SoM connector and carrier board connector combined height will be default 2mm (total height 5.6mm)or 2.5mm(total height 5.6mm) Note: tolerance ±0.2mm

OS:

OS version	Linux5.10.87+QT5.14.2		
Firmware installation	•SD / TF card		
	•U-disk		

Development board/kit



Carrier board features

Peripheral	QTY	Spec.		
		Dual asynchronous channels(8 data, 2clocks), supports 1920x1200p60; Available for below three modes:		
LVDS	2	•single LVDS output mode;		
	2	•2x single LVDS(copy) output mode: two LVDS output same content;		
		•dual LVDS output mode, 8-lane data and 2-lane clock combine to one output channel		
		Default and recommended model: Forlinx 10.1" LVDS module, 1280x800 @ 60fps		
RGR parallel	1	By FPC connector, 16-bit(RGB565)		
RGB parallel	1	Default and recommended model: Forlinx 7" LCD module, 1024x600@ 60fps		
Camera	1	FPC connector		
	1	Recommended module: OV5645, up to 2592X1944		
Ethernet	2	10/100/1000Mbps auto-negotiation, RJ45		
LICD2 O	4	3 x USB HOST		
USB2.0	4	1 x USB OTG		
DEDUC HART	2	UART0 of A53 and WKUP_UART0 of R5 converted to USB, by Type-C connector		
DEBUG UART	3	MCU_UART0 of M4F by 2.54mm pin headers		
DC405	1	Electrical isolated, automatic control of sending and receiving direction		
RS485	1	Static, surge, group pulse protection level-3		
CAN-FD	1	Electrical isolated, CAN-FD up to 5Mbps		
CAN-FD	2	Static, surge, group pulse protection level-3		
SPI	1	MCU_SPI0 by pin headers with pitch of 2.54mm		
SFI	1	Rating up to 50 MHz		
I2C	2	MCU_I2C0 and WKUP_I2C0 are by pin headers with pitch of 2.54mm		
GPMC	1	GPMC_AD0~AD15 by pin headers with pitch of 2.54mm, 16-bit data/ address signals and		
Grwc	1	related control signal		
Audio	1	1x earphone output and 1x MIC input		
TF-CARD	1	1x TF Card slot, supports UHS-I TF card, up to 104MB/s		
		4G and 5G are optional and alternative;		
4G/5G	1	4G: M.2 Key B 4G module, recommended model: Quectel EM05(default), EC20;		
40/30	1	5G: M.2 Key B 5G module, recommended model: Quectel RM500U-CN;		
		Standard MicroSIM card slot		
WiFi	1	On-boardAW-CM358M;		
D1		IEEE 802.11 a/b/g/n/ac dual-band WIFI, up to 433.3Mbps;		
Bluetooth	1	Bluetooth 5, up to 3Mbps		
KEY	5	4 keys input for A53, 1 key input for M4F		
LED	8	4 LED out put for A53, 4 LED output for M4F		
RTC	1	On-board separate RTC chip		
EEPROM	1	2K bit		
		Mounted to MCU_I2C0 or WKUP_I2C0		
QSPI Flash	1	128M bit		
QSF1 Flash		Mounted to A53 QSPI or MCU SPI0		
JTAG	1	By 2 x 10-Pin pin headers with pitch of 1.27mm		